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# Precision Monolithic Quad SPST CMOS Analog Switches

## FEATURES

- 44-V Supply Max Rating
- ±15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 25 Ω
- Fast Switching—$t_{ON}$: 110 ns
- Ultra Low Power—$P_D$: 0.35 μW
- TTL, CMOS Compatible
- Single Supply Capability

## BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

## APPLICATIONS

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Powered Systems
- Computer Peripherals

## DESCRIPTION

The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.35 μW) with high speed ($t_{ON}$: 110 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Vishay Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

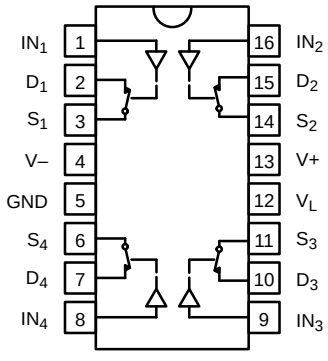
Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG411 and DG412 respond to opposite control logic as shown in the Truth Table. The DG413 has two normally open and two normally closed switches.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG411**

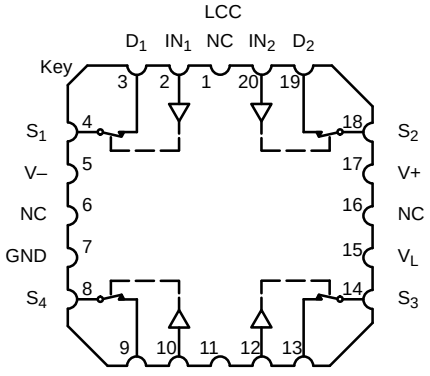
Dual-In-Line and SOIC




Top View

**DG411**

LCC




Top View

**TRUTH TABLE**

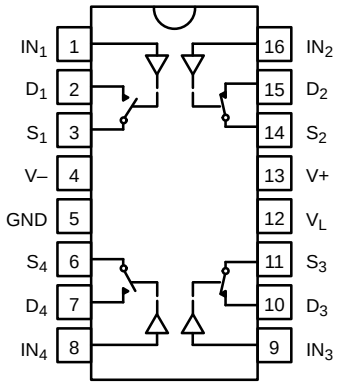
| Logic | DG411 | DG412 |
|---|---|---|
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG413**

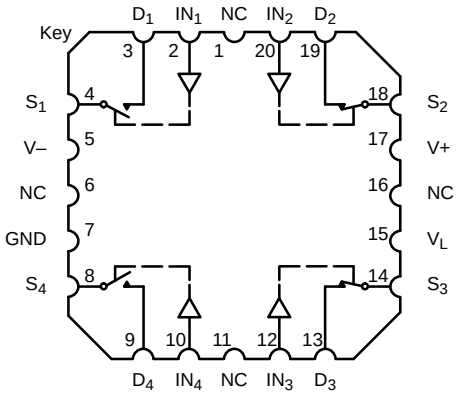
Dual-In-Line and SOIC




Top View

**DG413**

LCC




Top View

| TRUTH TABLE | | |
|---|---|---|
| **Logic** | **$SW_1$, $SW_4$** | **$SW_2$, $SW_3$** |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

| ORDERING INFORMATION | | |
|---|---|---|
| **Temp Range** | **Package** | **Part Number** |
| **DG411/412** | | |
| –40 to 85°C | 16-Pin Plastic DIP | DG411DJ |
| | | DG412DJ |
| –40 to 85°C | 16-Pin Narrow SOIC | DG411DY |
| | | DG412DY |
| –55 to 125°C | 16-Pin CerDIP | DG411AK, DG411AK/883, 5962-9073101MEA |
| | | DG412AK, DG412AK/883, 5962-9073102MEA |
| | LCC-20 | DG411AZ/883, 5962-9073101M2A |
| | | 5962-9073102M2A |
| **DG413** | | |
| –40 to 85°C | 16-Pin Plastic DIP | DG413DJ |
| | 16-Pin Narrow SOIC | DG413DY |
| –55 to 125°C | 16-Pin CerDIP | DG413AK, DG413AK/883, 5962-9073103MEA |
| | LCC-20 | 5962-9073103M2A |

## ABSOLUTE MAXIMUM RATINGS

V+ to V– ..... 44 V

GND to V– ..... 25 V

$V_L$ ..... (GND –0.3 V) to (V+) +0.3 V

Digital Inputs[a], $V_S$, $V_D$ ..... (V–) –2 V to (V+) +2 V
or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Peak Current, S or D (Pulsed 1 ms, 10% Duty Cycle) ..... 100 mA

Storage Temperature (AK, AZ Suffix) ..... –65 to 150°C
(DJ, DY Suffix) ..... –65 to 125°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] ..... 470 mW
16-Pin Narrow SOIC[d] ..... 600 mW
16-Pin CerDIP[e] ..... 900 mW
LCC-20[e] ..... 900 mW

Notes:
a. Signals on $S_X$, $D_X$, or $IN_X$ exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 25°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

## SPECIFICATIONS[a]

| Parameter | Symbol | Test Conditions Unless Specified<br>V+ = 15 V, V– = –15 V<br>$V_L$ = 5 V, $V_{IN}$ = 2.4 V, 0.8 V[f] | Temp[b] | Typ[c] | A Suffix –55 to 125°C<br>Min[d] | A Suffix –55 to 125°C<br>Max[d] | D Suffix –40 to 85°C<br>Min[d] | D Suffix –40 to 85°C<br>Max[d] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | Full | | –15 | 15 | –15 | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | V+ = 13.5 V, V– = –13.5 V<br>$I_S$ = –10 mA, $V_D$ = ±8.5 V | Room<br>Full | 25 | | 35<br>45 | | 35<br>45 | Ω |
| Switch Off Leakage Current | $I_{S(off)}$ | V+ = 16.5, V– = –16.5 V<br>$V_D$ = ±15.5 V, $V_S$ = ∓15.5 V | Room<br>Full | ±0.1 | –0.25<br>–20 | 0.25<br>20 | –0.25<br>–5 | 0.25<br>5 | nA |
| | $I_{D(off)}$ | | Room<br>Full | ±0.1 | –0.25<br>–20 | 0.25<br>20 | –0.25<br>–5 | 0.25<br>5 | |
| Channel On Leakage Current | $I_{D(on)}$ | V+ = 16.5 V, V– = –16.5 V<br>$V_S$ = $V_D$ = ±15.5 V | Room<br>Full | ±0.1 | –0.4<br>–40 | 0.4<br>40 | –0.4<br>–10 | 0.4<br>10 | |
| **Digital Control** | | | | | | | | | |
| Input Current, $V_{IN}$ Low | $I_{IL}$ | $V_{IN}$ Under Test = 0.8 V | Full | 0.005 | –0.5 | 0.5 | –0.5 | 0.5 | µA |
| Input Current, $V_{IN}$ High | $I_{IH}$ | $V_{IN}$ Under Test = 2.4 V | Full | 0.005 | –0.5 | 0.5 | –0.5 | 0.5 | |
| **Dynamic Characteristics** | | | | | | | | | |
| Turn-On Time | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF<br>$V_S$ = ±10 V See Figure 2 | Room<br>Full | 110 | | 175<br>240 | | 175<br>220 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | 100 | | 145<br>160 | | 145<br>160 | |
| Break-Before-Make Time Delay | $t_D$ | DG413 Only, $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | Room | 25 | | | | | |
| Charge Injection | Q | $V_g$ = 0 V, $R_g$ = 0 Ω, $C_L$ = 10 nF | Room | 5 | | | | | pC |
| Off Isolation[e] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF,<br>f = 1 MHz | Room | 68 | | | | | dB |
| Channel-to-Channel Cross-talk[e] | $X_{TALK}$ | | Room | 85 | | | | | |
| Source Off Capacitance[e] | $C_{S(off)}$ | f = 1 MHz | Room | 9 | | | | | pF |
| Drain Off Capacitance[e] | $C_{D(off)}$ | | Room | 9 | | | | | |
| Channel On Capacitance[e] | $C_{D(on)}$ | | Room | 35 | | | | | |
| **Power Supplies** | | | | | | | | | |
| Positive Supply Current | I+ | V+ = 16.5, V– = –16.5 V<br>$V_{IN}$ = 0 or 5 V | Room<br>Full | 0.0001 | | 1<br>5 | | 1<br>5 | µA |
| Negative Supply Current | I– | | Room<br>Full | –0.0001 | –1<br>–5 | | –1<br>–5 | | |
| Logic Supply Current | $I_L$ | | Room<br>Full | 0.0001 | | 1<br>5 | | 1<br>5 | |
| Ground Current | $I_{GND}$ | | Room<br>Full | –0.0001 | –1<br>–5 | | –1<br>–5 | | |

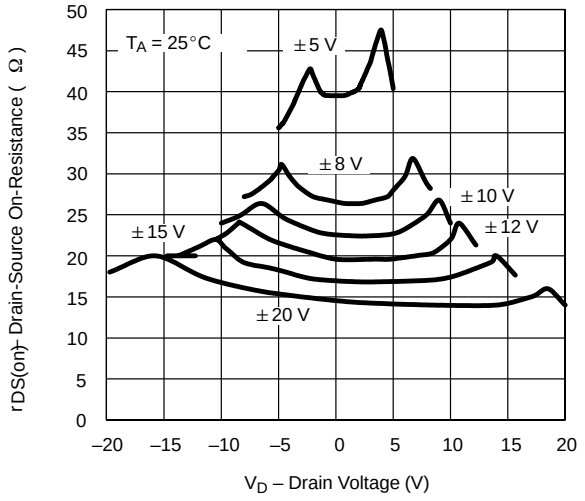
## SPECIFICATIONS[a] FOR UNIPOLAR SUPPLIES

| Parameter | Symbol | Test Conditions Unless Specified<br>V+ = 12 V, V– = 0 V<br>$V_L$ = 5 V, $V_{IN}$ = 2.4 V, 0.8 V[f] | Temp[b] | Typ[c] | A Suffix –55 to 125°C Min[d] | A Suffix –55 to 125°C Max[d] | D Suffix –40 to 85°C Min[d] | D Suffix –40 to 85°C Max[d] | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | |
| Analog Signal Range[e] | $V_{ANALOG}$ | | Full | | | 12 | | 12 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | V+ = 10.8 V, $I_S$ = –10 mA<br>$V_D$ = 3 V, 8 V | Room<br>Full | 40 | | 80<br>100 | | 80<br>100 | Ω |
| **Dynamic Characteristics** | | | | | | | | | |
| Turn-On Time | $t_{ON}$ | $R_L$ = 300 Ω, $C_L$ = 35 pF<br>$V_S$ = 8 V, See Figure 2 | Room<br>Hot | 175 | | 250<br>400 | | 250<br>315 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Hot | 95 | | 125<br>140 | | 125<br>140 | |
| Break-Before-Make Time Delay | $t_D$ | DG413 Only, $V_S$ = 8 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF | Room | 25 | | | | | |
| Charge Injection | Q | $V_g$ = 6 V, $R_g$ = 0 Ω, $C_L$ = 10 nF | Room | 25 | | | | | pC |
| **Power Supplies** | | | | | | | | | |
| Positive Supply Current | I+ | V+ = 13.5, $V_{IN}$ = 0 or 5 V | Room<br>Hot | 0.0001 | | 1<br>5 | | 1<br>5 | µA |
| Negative Supply Current | I– | | Room<br>Hot | –0.0001 | –1<br>–5 | | –1<br>–5 | | |
| Logic Supply Current | $I_L$ | | Room<br>Hot | 0.0001 | | 1<br>5 | | 1<br>5 | |
| Ground Current | $I_{GND}$ | | Room<br>Hot | –0.0001 | –1<br>–5 | | –1<br>–5 | | |

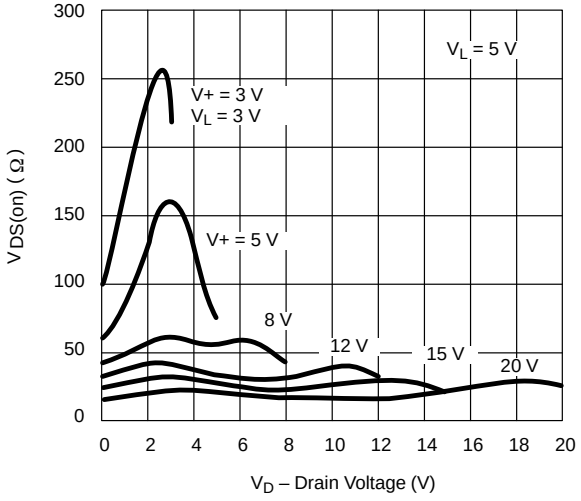
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

**On-Resistance vs. $V_D$ and Power Supply Voltage**

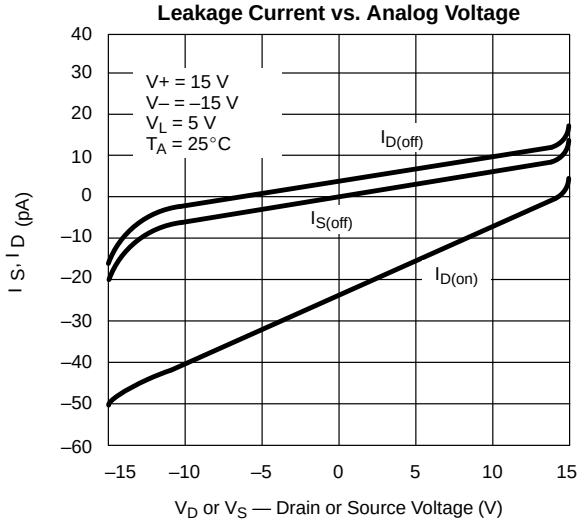



**On-Resistance vs. $V_D$ and Unipolar Supply Voltage**

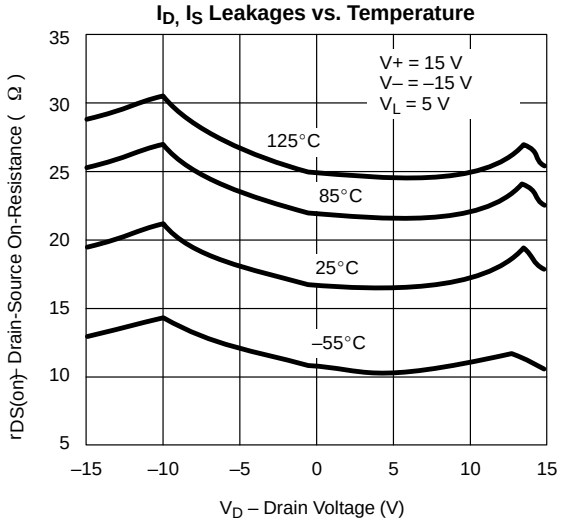


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

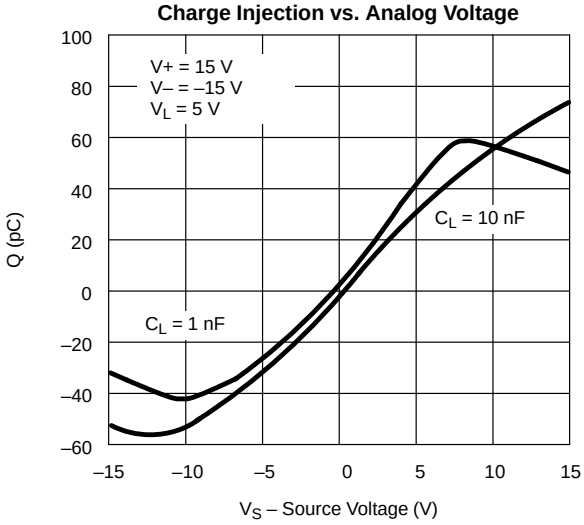
**Leakage Current vs. Analog Voltage**



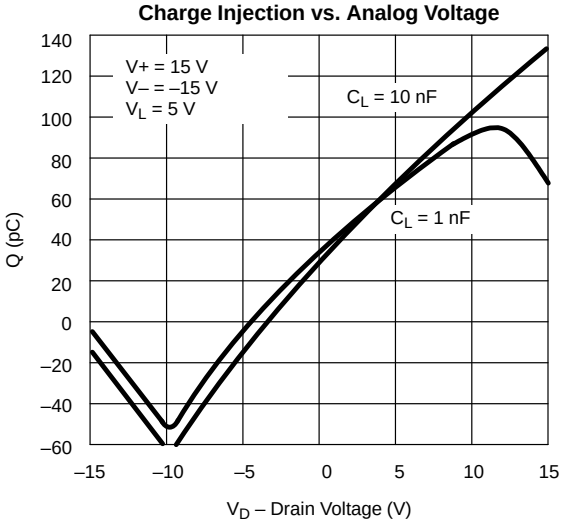

**$I_D$, $I_S$ Leakages vs. Temperature**



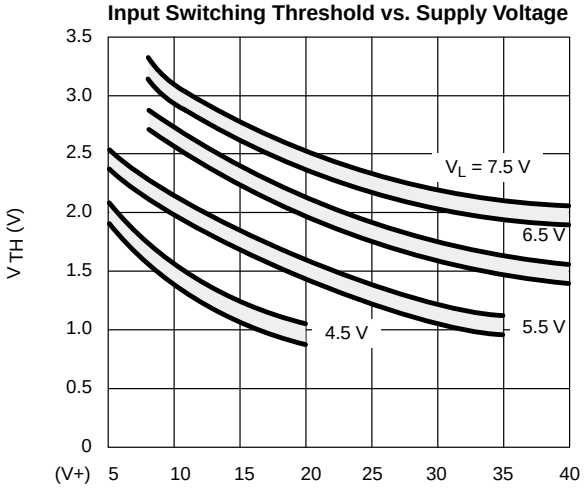

**Charge Injection vs. Analog Voltage**



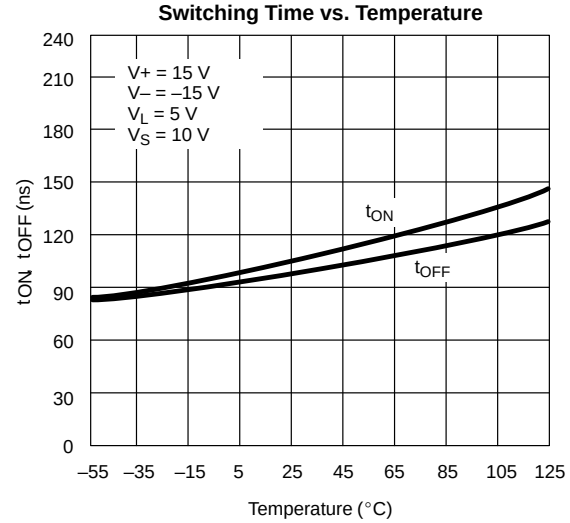

**Charge Injection vs. Analog Voltage**



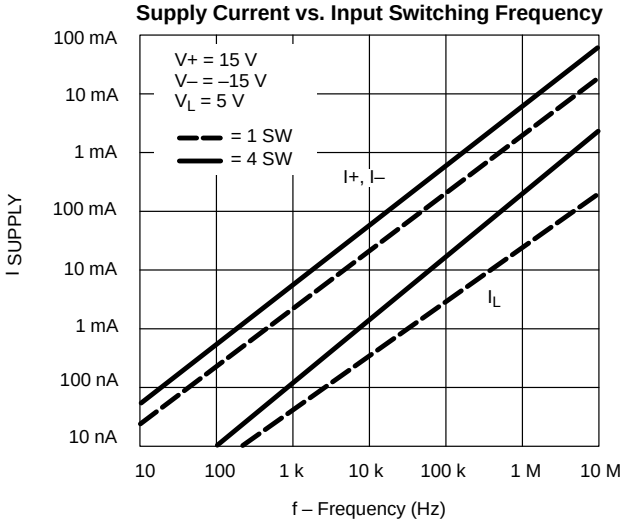

**Input Switching Threshold vs. Supply Voltage**




**Switching Time vs. Temperature**



## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)




## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

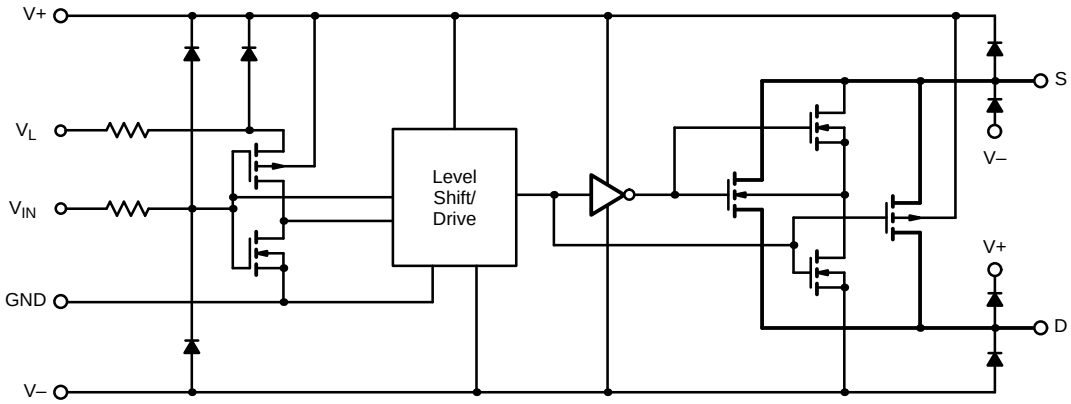
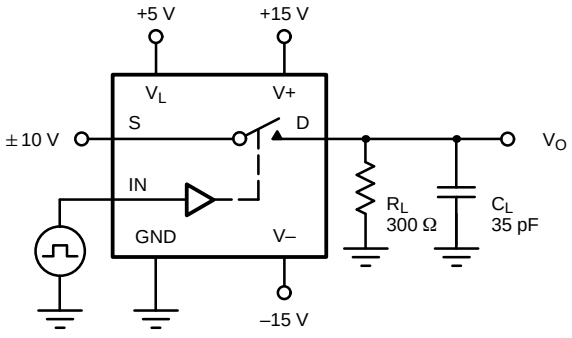


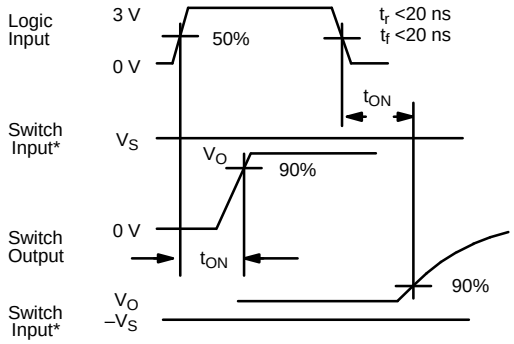

**FIGURE 1.**

## TEST CIRCUITS




$C_L$ (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

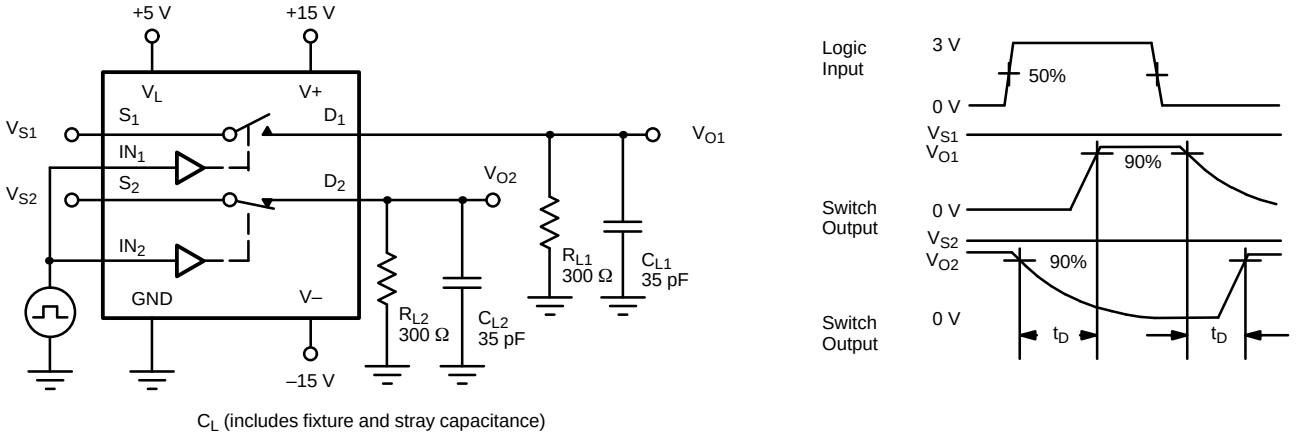



*$V_S$ = 10 V for $t_{ON}$, $V_S$ = –10 V for $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

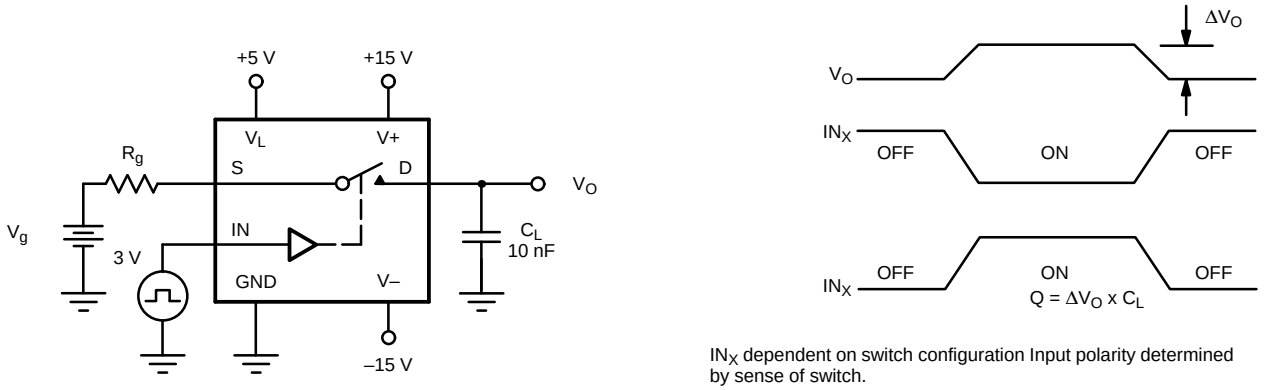
**FIGURE 2.** Switching Time

## TEST CIRCUITS




$C_L$ (includes fixture and stray capacitance)

**FIGURE 3.** Break-Before-Make (DG413)




$IN_X$ dependent on switch configuration Input polarity determined by sense of switch.

**FIGURE 4.** Charge Injection

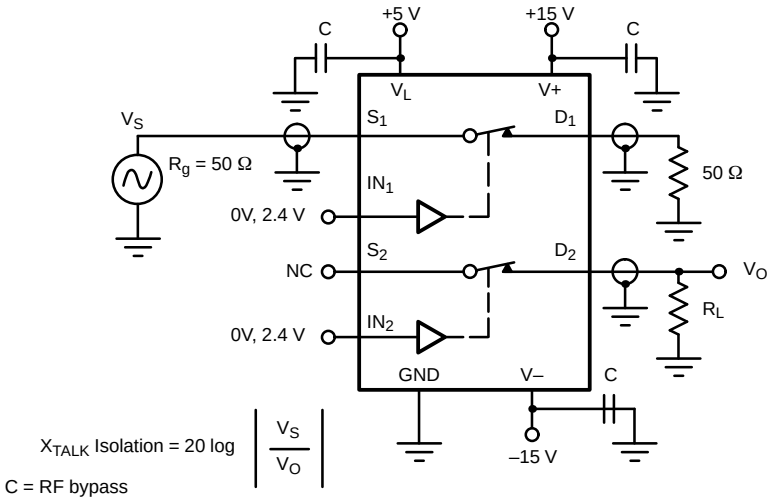



**FIGURE 5.** Crosstalk

## TEST CIRCUITS

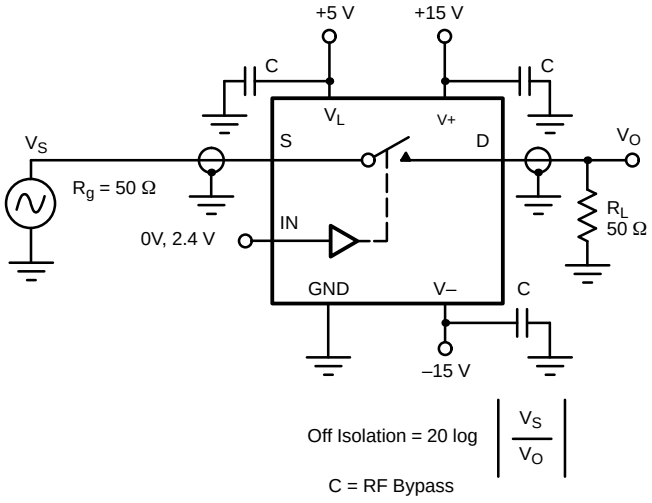



**FIGURE 6.** Off Isolation

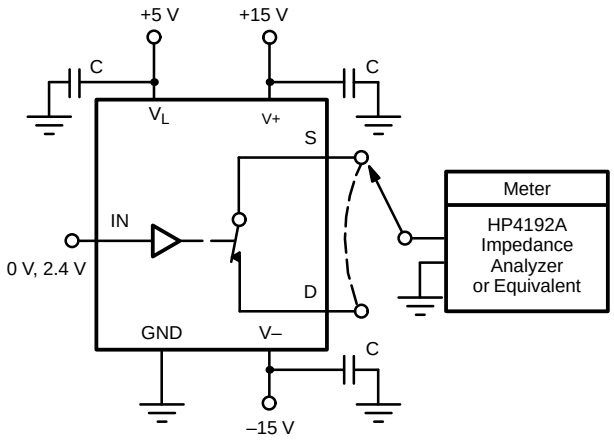



**FIGURE 7.** Source/Drain Capacitances

## APPLICATIONS

### Single Supply Operation:

The DG411/412/413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V+ is tied to $V_L$ and V– is tied to 0 V. See Input Switching Threshold vs. Supply Voltage curve for $V_L$ versus input threshold requirments.

### Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

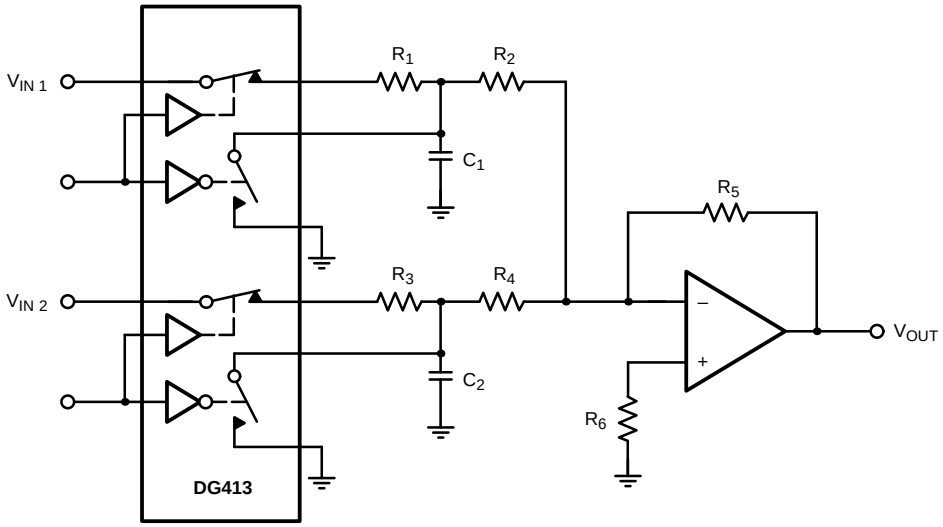



**FIGURE 8.** Summing Amplifier